CLAIMS:

1. An instruction controlled data processing device, the device comprising

- an instruction issue unit (10), having an issue slot (11) for issuing instructions from an instruction set, the instruction issue unit issuing respective ones of the instructions in successive instruction cycles;
- a register file (14) with an read port and a write port;
- a group (12) of functional units (20a,b), each functional unit (20a,b) having a control input coupled to the issue slot (11), an operand input (22a,b) coupled to the read port and a result output coupled to the write port, each functional unit (20a,b) being arranged to respond to instructions from a respective sub-set of the instruction set to which the other functional units (20a,b) do not respond, the instruction set further comprising a combination instruction to which a first and second one of the functional units (20a,b) respond;
- a control unit (28) coupled to the issue slot (11) and responsive to the combination instruction from the instruction set, to route the result output of the first one of the functional units (20a) to the operand input of the second one of the functional units (20b).

2. An instruction controlled data processing device according to Claim 1, organized as a VLIW processor, the issue slot (11) being one of a plurality of issue slots of the instruction issue unit for issuing a VLIW instruction word that contains the combination instruction as one of its instructions, the register file (14) having a plurality of sets of read and write ports, the device comprising respective functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports for executing respective instructions from the VLIW instruction word, the first and second one of the functional units in responding to the combination instruction issued in the issue slot in parallel with execution of instructions issued in the same instruction word as the combination instruction.

3. An instruction controlled data processing device according to Claim 1, wherein the first and second one of the functional units (20a,b) respond to the combination instruction in a same instruction execution cycle.

4. An instruction controlled data processing device according to Claim 3, comprising a clock circuit (16) for clocking the instruction cycles, the clock circuit (16) having a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate within an instruction execution cycle the latency involved in producing a result from the second one of the functional units (20b) in response to an operand applied to the first one of the functional units (20a) also during execution of the combination instruction within the instruction execution cycle, and a second clock rate that is too fast to accommodate said latency in the instruction cycle, but accommodates latency of instructions from said sub-sets.

5. An instruction controlled data processing device according to Claim 1, wherein the instruction issue unit (10) has a further issue slot and the register file (14) has a further read port, the device comprising a further functional unit (40b) having a control input coupled to the further issue slot and an operand input coupled to the further read port, the control unit (28) being arranged to route the result output of the further functional units (40b) to a further operand input of the second one of the functional units (20b) under control of the combination instruction, bypassing the register file (14) under control of the combination instruction.

6. An instruction controlled data processing device according to Claim 5, programmed with a program that contains a VLIW instruction that contains a command for the further functional unit (40b) and the combination instruction for the group of functional units (12) for issue in a same instruction cycle.

7. An instruction controlled data processing device according to Claim 1, wherein the control unit (28) is arranged to make the second one of the functional units (20b) respond to the combination instruction in an instruction execution cycle following an instruction execution cycle in which the first one of the functional units (20a) responds to the combination instruction.

8. An instruction controlled data processing device according to Claim 7, wherein the result of the first one of the functional units (20a) is routed without intermediate

latching from the first one of the functional units (20a) to the operand input of the second one of the functional units (20b).

9. A method of executing a processing task, the method comprising
- providing a group of functional units (12),
- issuing successive instructions to the group (12);
- executing those of the instructions that are of a first type each with an individual one of the functional units (20a,b),
- executing an instructions that is of a second type with a first and a second one of the functional units in series (20a,b);
- routing a result of the first one of the functional units (20a) to an operand of the second one of the functional units (20b) in response to the instruction of the second type.

10. A method according to Claim 9, wherein the first and the second one of the functional units (20a,b) respond to the instruction of the second type in a same instruction execution cycle, the method comprising
- selecting an instruction cycle rate from at least a first and second rate, the first rate being so slow that execution of a combination instruction by a cascade of at least two of the functional units (20a,b) fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions by single ones of the functional units fits within the instruction execution cycle at the second rate, execution of the combination instruction not fitting within one instruction execution cycle at the second rate;
- adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the combination instruction is used when the task is executed at the first rate and the combination instruction is replaced by instructions of the first type with corresponding effect when the task is executed at the second rate.

11. A method according to Claim 9, comprising
- issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units (40a,b);
- including in the instruction word that contains the instruction of the second type an further instruction for a particular one of the further functional units (40a,b);

- routing a further result of the further instruction from the particular one of the further functional units (40a,b) to a further operand input of the second one of the functional units (20b) in response to the instruction of the second type.